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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/871,277	MA ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,55-73 and 90-114* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-17,55-61,63-71, 73, 90-109, and 111-114* is/are rejected.

7)☒ Claim(s) *8,18,62,72 and 110* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/13/04 and 8/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-2, 4-5, 9-12, 14-15, 55-56, 58-59, 63-66, 68-69, 73, 90-93, 95, 100, 102-104, 106-107, and 111-114 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Powell, Jr. et al. (U.S. Patent No. 5,896,516) and Foster et al. (U.S. Patent No. 6,038,630).

Referring to claim 1: Powell discloses a crossbar including an input sorting unit (figure 2, combined structures 34, 52, and 36) associated with one input interface; and the input sorting unit capable of receiving from a respective peripheral device an access request to any one of a plurality of peripheral devices. Powell's crossbar further includes a merge and interleave unit (figure 2, structures 44, 46, and 58) associated with one output interface; and the merge and interleave unit is capable of arbitrating among competing access requests and selects one of the

competing access requests and forwarding the selected request to the designated peripheral device. Powell discloses that the crossbar includes a plurality of I/O ports, each port having associated input and output buffers for sorting and merging (figure 1). Thus, Powell discloses a crossbar with a plurality of input sorting units and a plurality of merge and interleave unit. In addition, the court (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8) has held that the duplication of the essential working parts of device involves only routine skill in the art.

Powell does not disclose that the designated device is a memory device. Foster discloses that it is known to use a crossbar to distribute the memory access request (abstract, figure 3). Foster teaches one to employ a crossbar to share access control for an integrated system which allows multiple functions of the integrated system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach (column 2, lines 4-10).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Foster's teaching onto the Powell because Foster teaches one to arbitrate memory access via a crossbar system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach.

Referring to claim 2: Powell discloses the translation circuit (figure 2, structure 32) and wherein the input sorting unit receives the access requests through the translation circuit.

Referring to claim 4: Powell discloses buffers for buffering the access requests (figure 2, structure 34).

Referring to claim 5: The FIFO is a well-known practice as disclosed in the Application (page 4, first paragraph).

Referring to claim 9: Powell discloses a plurality of read buffers (figure 1, structure output buffer, figure 2, structure 46) capable of receiving and buffering read data. Powell further discloses an output management unit (figure 2, structure 48) capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

Referring to claim 10: Foster teaches one to arbitrate memory access via a crossbar, and the connecting means to the memory is the memory interface.

Referring to claim 11: Powell discloses a crossbar including an input sorting unit (figure 2, combined structures 34, 52, and 36) associated with one input interface; and the input sorting unit capable of receiving from a respective peripheral device an access request to any one of a plurality of peripheral devices. Powell's crossbar further includes a merge and interleave unit (figure 2, structures 44, 46, and 58) associated with one output interface; and the merge and interleave unit is capable of arbitrating among competing access requests and selects one of the competing access requests and forwarding the selected request to the designated peripheral device. Powell discloses that the crossbar includes a plurality of I/O ports, each port having associated input and output buffers for sorting and merging (figure 1). Thus, Powell discloses a crossbar with a plurality of input sorting units and a plurality of merge and interleave unit. In addition, the court (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8) has held that the duplication of the essential working parts of device involves only routine skill in the art.

Powell does not disclose that the designated device is a memory device. Foster discloses that it is known to use a crossbar to distribute the memory access request (abstract, figure 3). Foster teaches one to employ a crossbar to share access control for an integrated system which allows multiple functions of the integrated system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach (column 2, lines 4-10).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Foster's teaching onto the Powell because Foster teaches one to arbitrate memory access via a crossbar system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach.

Referring to claim 12: Foster teaches one to arbitrate memory access via a crossbar, and the connecting means to the memory is the memory interface.

Referring to claim 14: Powell discloses buffers for buffering the access requests (figure 2, structure 34).

Referring to claim 15: The FIFO is a well-known practice as disclosed in the Application (page 4, first paragraph).

Referring to claim 55: Powell discloses a crossbar including an input sorting unit (figure 2, combined structures 34, 52, and 36) associated with one input interface; and the input sorting unit capable of receiving from a respective peripheral device an access request to any one of a plurality of peripheral devices. Powell's crossbar further includes a merge and interleave unit (figure 2, structures 44, 46, and 58) associated with one output interface; and the merge and

interleave unit is capable of arbitrating among competing access requests and selects one of the competing access requests and forwarding the selected request to the designated peripheral device. Powell discloses that the crossbar includes a plurality of I/O ports, each port having associated input and output buffers for sorting and merging (figure 1). Thus, Powell discloses a crossbar with a plurality of input sorting units and a plurality of merge and interleave unit. In addition, the court (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8) has held that the duplication of the essential working parts of device involves only routine skill in the art.

Powell does not disclose that the designated device is a memory device. Foster discloses that it is known to use a crossbar to distribute the memory access request (abstract, figure 3). Foster teaches one to employ a crossbar to share access control for an integrated system which allows multiple functions of the integrated system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach (column 2, lines 4-10).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Foster's teaching onto the Powell because Foster teaches one to arbitrate memory access via a crossbar system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach.

Referring to claim 56: Powell discloses the translation circuit (figure 2, structure 32), which is a Glue logic unit, and wherein the input sorting unit receives the access requests through the translation circuit.

Referring to claim 58: Powell discloses buffers for buffering the access requests (figure 2, structure 34).

Referring to claim 59: The FIFO is a well-known practice as disclosed in the Application (page 4, first paragraph).

Referring to claim 63: Powell discloses a plurality of read buffers (figure 1, structure output buffer, figure 2, structure 46) capable of receiving and buffering read data. Powell further discloses an output management unit (figure 2, structure 48) capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

Referring to claim 64: Foster teaches one to arbitrate memory access via a crossbar, and the connecting means to the memory is the memory interface.

Referring to claim 65: Powell discloses a crossbar including an input sorting unit (figure 2, combined structures 34, 52, and 36) associated with one input interface; and the input sorting unit capable of receiving from a respective peripheral device an access request to any one of a plurality of peripheral devices. Powell's crossbar further includes a merge and interleave unit (figure 2, structures 44, 46, and 58) associated with one output interface; and the merge and interleave unit is capable of arbitrating among competing access requests and selects one of the competing access requests and forwarding the selected request to the designated peripheral device. Powell discloses that the crossbar includes a plurality of I/O ports, each port having associated input and output buffers for sorting and merging (figure 1). Thus, Powell discloses a crossbar with a plurality of input sorting units and a plurality of merge and interleave unit. In

addition, the court (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8) has held that the duplication of the essential working parts of device involves only routine skill in the art.

Powell does not disclose that the designated device is a memory device. Foster discloses that it is known to use a crossbar to distribute the memory access request (abstract, figure 3). Foster teaches one to employ a crossbar to share access control for an integrated system which allows multiple functions of the integrated system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach (column 2, lines 4-10).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Foster's teaching onto the Powell because Foster teaches one to arbitrate memory access via a crossbar system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach.

Referring to claim 66: Foster teaches one to arbitrate memory access via a crossbar, and the connecting means to the memory is the memory interface.

Referring to claim 68: Powell discloses buffers for buffering the access requests (figure 2, structure 34).

Referring to claim 69: The FIFO is a well-known practice as disclosed in the Application (page 4, first paragraph).

Referring to claim 73: Powell discloses a plurality of read buffers (figure 1, structure output buffer, figure 2, structure 46) capable of receiving and buffering read data. Powell further discloses an output management unit (figure 2, structure 48) capable of receiving read data from

the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

Referring to claim 90: Powell discloses a crossbar including an input sorting unit (figure 2, combined structures 34, 52, and 36) associated with one input interface; and the input sorting unit capable of receiving from a respective peripheral device an access request to any one of a plurality of peripheral devices. Powell's crossbar further includes a merge and interleave unit (figure 2, structures 44, 46, and 58) associated with one output interface; and the merge and interleave unit is capable of arbitrating among competing access requests and selects one of the competing access requests and forwarding the selected request to the designated peripheral device. Powell discloses that the crossbar includes a plurality of I/O ports, each port having associated input and output buffers for sorting and merging (figure 1). Thus, Powell discloses a crossbar with a plurality of input sorting units and a plurality of merge and interleave unit. In addition, the court (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8) has held that the duplication of the essential working parts of device involves only routine skill in the art.

Powell does not disclose that the designated device is a memory device. Foster discloses that it is known to use a crossbar to distribute the memory access request (abstract, figure 3). Foster teaches one to employ a crossbar to share access control for an integrated system which allows multiple functions of the integrated system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach (column 2, lines 4-10).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Foster's teaching onto the Powell because Foster

teaches one to arbitrate memory access via a crossbar system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach.

Referring to claim 91: Foster teaches one to arbitrate memory access via a crossbar, and the connecting means to the memory is the memory interface.

Referring to claim 92: Powell discloses a plurality of read buffers (figure 1, structure output buffer, figure 2, structure 46) capable of receiving and buffering read data. Powell further discloses an output management unit (figure 2, structure 48) capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

Referring to claim 93: Powell discloses the translation circuit (figure 2, structure 32) and wherein the input sorting unit receives the access requests through the translation circuit.

Referring to claim 95: The data transmitted in the Powell's crossbar is the plurality of characteristics for the access requests.

Referring to claim 100: Foster teaches one to arbitrate memory access via a crossbar, and the connecting means to the memory is the memory interface.

Referring to claims 102-103: Powell discloses a crossbar including an input sorting unit (figure 2, combined structures 34, 52, and 36) associated with one input interface; and the input sorting unit capable of receiving from a respective peripheral device an access request to any one of a plurality of peripheral devices. Powell's crossbar further includes a merge and interleave unit (figure 2, structures 44, 46, and 58) associated with one output interface; and the merge and interleave unit is capable of arbitrating among competing access requests and selects one of the

competing access requests and forwarding the selected request to the designated peripheral device. Powell discloses that the crossbar includes a plurality of I/O ports, each port having associated input and output buffers for sorting and merging (figure 1). Thus, Powell discloses a crossbar with a plurality of input sorting units and a plurality of merge and interleave unit. In addition, the court (St. Regis Paper Co. v. Bemis Co., 193 USPQ 8) has held that the duplication of the essential working parts of device involves only routine skill in the art.

Powell does not disclose that the designated device is a memory device. Foster discloses that it is known to use a crossbar to distribute the memory access request (abstract, figure 3). Foster teaches one to employ a crossbar to share access control for an integrated system which allows multiple functions of the integrated system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach (column 2, lines 4-10).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Foster's teaching onto the Powell because Foster teaches one to arbitrate memory access via a crossbar system to simultaneously access different external devices through multiple ports avoiding the performance degradation and increased cost inherent in a separate, dedicated port approach.

Referring to claim 104: Powell discloses the translation circuit (figure 2, structure 32) and wherein the input sorting unit receives the access requests through the translation circuit.

Referring to claim 106: Powell discloses buffers for buffering the access requests (figure 2, structure 34).

Referring to claim 107: The FIFO is a well-known practice as disclosed in the Application (page 4, first paragraph).

Referring to claims 111-112: Powell discloses a plurality of read buffers (figure 1, structure output buffer, figure 2, structure 46) capable of receiving and buffering read data. Powell further discloses an output management unit (figure 2, structure 48) capable of receiving read data from the read buffers and forwarding the received read data to a respective one of the devices that generated the access request associated with the read data.

Referring to claims 113-114: Foster teaches one to arbitrate memory access via a crossbar, and the connecting means to the memory is the memory interface.

4. Claims 3 and 13, 57, 67, 94, 105 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Powell, Foster, and Berglund et al. (U.S. Patent No. 4,258,417).

Referring to claims 3, 13, 57, 67, 94, and 105: Powell's crossbar will forward commands and data from each peripheral device (column 3, line 1) and the associated address (column 3, lines 6-7). Powell's command is the opcode, but Powell does not explicitly disclose the virtual address. Berglund discloses how to access memory, and teaches that each requested memory address is a virtual address and the address translation is needed (column 2, lines 52-56). Berglund further discloses that command decoder is a known practice to control memory access operations, FETCH and STORE (column 10, lines 52-56). Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Berglund's teaching onto Powell and

Foster because Berglund teaches one on how to translate the correct address and command in order to access the memory.

5. Claims 6, 16, 60, 70, and 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Powell, Foster, and Bitner (U.S. Patent No. 5,210,829) or the combination of Powell, Foster, and Crouse et al. (U.S. Patent No. 5,309,426).

Referring to claims 6, 16, and 60, 70: Powell does not disclose the stalling. Bitner discloses a buffer threshold mechanism that will stall the host when the buffer is full (column 3, lines 43-48). Crouse discloses a high performance switch, which will reject the control message if the buffer is full; the rejection is the stalling. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Bitner and Crouse's teaching on stalling because they teaches one to prevent the loss of data when the buffer is full.

6. Claims 7, 17, 61, 71, 95, 96-100, and 109 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Powell, Foster, and Schlotterer (U.S. Patent No. 4,130,864).

Referring to claims 7, 17, 61, 71, 96-98, and 109: Powell discloses a priority compare circuit (figure 2, structure 44) for capable of comparing the composite request priorities and selecting one access request. Although Powell does not explicitly disclose a request multiplexer controlled by the priority compare circuit to output the selected access request, Powell's compare circuit receives requests from ports 1 to 9 (figure 1, figure 2's structure 59). Thus, the port receiving part of the compare circuit is the multiplexer, and the circuit's selecting decision

controls the output of the multiplexer. Powell discloses commands and data (column 3, line 1), which are the operational characteristics and characteristics for the access request. Powell does not explicitly disclose a means for generating priority. Foster discloses an arbitrator (figure 3, structure 235), but Foster does not explicitly disclose how to generate priority.

Schlotterer discloses a priority selection circuit for a multiported functional unit. Schlotterer teaches that it is known to apply different priority scheme to generate the priority order (column 1, lines 27-55). Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Schlotterer's teaching to Powell and Foster because Schlotterer teaches one on how to determine/set the priority of the access request.

Referring to claim 99: Schlotterer discloses different approaches of assigning weight (column 1, lines 27-55), which is the programming of assigned weight factor before assigning.

Referring to claim 100: Schlotterer discloses the rotational priority, which that each selected request will be put on the button of the list, and advance rest of the node to one step close to the selected status, which is the increasing the composite request priority of each access request not selected or decreasing the composite request priority of the selected request.

Allowable Subject Matter

7. Claims 8, 18, 62, 72, and 110 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior arts on the record do not explicitly disclose the claimed structures and the combined means.

Response to Arguments

9. In response to Applicant's assertion that the "a buffer" in original claim 14 is a *clearly* different buffer from the parent claim 11's "a read buffer": Examiner strongly disagrees. The "buffer" is a broader term than the "read buffer"; thus, they are not mutually exclusive, the "read buffer" is within the scope of the "buffer", and the "a buffer" in original claim 14 is never a *clearly* different buffer from the parent claim 11's "a read buffer". Nevertheless, the associated 112 Rejection is withdrawn based on amending the "a buffer" to "a request buffer".

10. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant argues that Examiner has not made any factual basis to supply the admitted deficiencies of Powell (Remark, page 17, last paragraph). However, Applicant fails to point out which admitted deficiencies are not taught by either the prior art Foster or judicial notice or MPEP 2144 from the 103(a) Rejection. Applicant further asserts that the reliance on MPEP 2144 is improper (Remark, page 17, last line) and recites a case law in re Ochiai, but Applicant fails to point out why the MPEP 2144 is improper applied and how the cited case law supports Applicant's allegation.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 703-305-4571. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-308-3110. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin King
September 27, 2004

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